IN THE CLAIMS

1. (currently amended) A packet data processing apparatus for processing a packet received from a network by a processor, comprising:

a packet data access part, which has a plurality of registers arranged in series, shifting the received packet through the plurality of registers toward an outlet in synchronization with a clock,

wherein:

the processor processes the received packet while the received packet is being shifted through the plurality of registers, independently of an instruction order for processing the received packet;

the processor and the packet data access part are directly connected by a read data line and a write data line;

the processor reads out or writes data from or to the packet data access part by synchronizing the cycle time of the processor by the read data line and the write data line; and

each of the plurality of registers of the packet data access part is connected to a neighbor register via a selector which selects write data from the processor or the neighbor register, so as to enable the processor to process the received packet, instead of fully shifting the received packet through the entire series of registers.

2. (original) The packet data processing apparatus as claimed in claim 1, further comprising:

an intermediate data maintaining part, which has a plurality of registers arranged in series, sequentially shifting intermediate data showing a process result of the received packet through the plurality of registers toward the outlet in synchronization with the clock.

3. (original) The packet data processing apparatus as claimed in claim 1, further comprising a search table, wherein said processor searches the search table by using data of the received packet, and retrieves information corresponding to the data of the received packet.

4. (original) The packet data processing apparatus as claimed in claim 1, wherein said processor processes the received packet being shifter by said packet data access part in accordance with a set of instructions.

5. (original) The packet data processing apparatus as claimed in claim 4, wherein the set of sequential instructions is for executing a checksum calculation for the received packet.

6. (original) The packet data processing apparatus as claimed in claim 4, wherein the set of sequential instructions is for executing a Time-To-Live calculation for the received packet.

7. (original) The packet data processing apparatus as claimed in claim 1, further comprising a search table, wherein said processor searches said search table for transmission interface information by using a destination address stored in the received packet, and retrieves the transmission interface information corresponding to the destination address, in accordance with a set of instructions for forwarding the received packet to the destination address while the

received packet is shifted by said packet data access part.

8. (currently amended) A packet relay apparatus for forwarding a packet received from a network, comprising:

a plurality of processors being connected in series in that the packet sequentially passes through the plurality of processors, each processor comprising:

a packet data access part, which has a plurality of registers arranged in series, shifting the received packet through the plurality of registers toward an outlet in synchronization with a clock,

wherein:

the processor processes the received packet while the received packet is being shifted through the plurality of registers, independently of an instruction order for processing the received packet;

the processor and the packet data access part are directly connected by a read data line and a write data line;

the processor reads out or writes data from or to the packet data access part by synchronizing the cycle time of the processor by the read data line and the write data line; and

each of the plurality of registers of the packet data access part is connected to a neighbor register via a selector which selects write data from the processor or the neighbor register, so as to enable the processor to process the received packet, instead of fully shifting the received packet through the entire series of registers.

9. (original) The packet relay apparatus as claimed in claim 8, wherein each processor independently processes the received packet being shifted by said packet data access part ins accordance with a different instruction order.

10. (previously presented) The packet relay apparatus as claimed in claim 8, further comprising:

a shared data access part, which has at least one register to be shared, capable of being accessed by the plurality of processors connected in series.

11. (original) The packet data processing apparatus as claimed in claim 1, further comprising:

a write-position changing part changing a write-position of said plurality of registers of the packet data access part where the write-position defines an inlet point at which said packet data access part received the packet from an exterior thereof.

12. (original) The packet data processing apparatus as claimed in claim 1, further comprising:

a send-position changing part changing a send-position of said plurality of registers of the packet data access part where the send-position defines an outlet point at which said packet data access point sends the packet to an exterior thereof.